EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	2	(intellectual adj propertY IP) and semiconductor with wiring with substrate and boundary adj scan and (On adj Super adj Sub IPOS)	USPAT	OR	ON	2006/06/09 17:13
S2	2	semiconductor adj device and (intellectual adj propertY IP) and semiconductor with wiring with substrate and boundary adj scan and (On adj Super adj Sub IPOS)	USPAT	OR	ON	2006/06/09 17:13
S5	18	(intellectual adj propertY IP) and semiconductor with substrate and (On adj Super adj Sub IPOS)	USPAT	OR	ON	2006/06/09 17:14
S6	45	(intellectual adj propertY IP) with (On adj Super adj Sub IPOS)	USPAT	OR	ON	2006/06/09 17:15
S7	45	(intellectual adj propertY IP) with (On adj Super-Sub IPOS)	USPAT	OR	ON	2006/06/09 17:17
S9	45	(intellectual adj propertY IP) with (On adj Super-Sub IPOS)	USPAT	OR	ON	2006/06/09 17:18
S4	2	(intellectual adj propertY IP) and semiconductor with substrate and boundary adj scan and (On adj Super adj Sub IPOS)	USPAT	OR	ON	2006/06/09 17:19
S11	31	(intellectual adj property IP) and semiconductor with substrate and boundary adj scan	USPAT	OR	ON	2006/06/09 17:21
S12	2	(intellectual adj property IP) and semiconductor with substrate and boundary adj scan and (linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR)	USPAT	OR	ON	2006/06/09 17:22
S13	3	(intellectual adj property IP) and boundary adj scan and (linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR)	USPAT	OR	ON	2006/06/09 17:23
S15	158	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR)	USPAT	OR	ON	2006/06/09 17:25
S17	120	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan	USPAT	OR	ON	2006/06/09 17:28

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S16	158	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR)	USPAT	OR	ON	2006/06/09 17:28
S14	6	(intellectual adj property IP) and (linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR)	USPAT	OR	ON	2006/06/09 17:28
S18	37	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and TAP	USPAT	OR	ON	2006/06/09 17:30
S19	59	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller	USPAT	OR	ON	2006/06/09 17:32
S20	53	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:33
S22	46	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller and BIST and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:34
S21	48	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller and $1BIST and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:34
S25	2	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller and BIST and (intellectual adj propertY IP) and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:36
S24	46	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller and BIST and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:36
S26	4	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller and BIST and (intellectual adj propertY IP) and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 17:39

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S28	32	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) and scan and controller and BIST and core and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 17:43
S27	36	(linear adj feedback adj shift adj register LFSR) and (multiple adj input adj signature adj register MISR) and scan and controller and BIST and core and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 17:43
S31	18	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) with scan and BIST and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 17:50
S30	4	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) with scan and BIST and core and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 17:50
S35	6	(intellectual adj propertY IP) with (On adj Super-Sub IPOS) and chip and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:55
S33	41	(intellectual adj propertY IP) with (On adj Super-Sub IPOS) and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:55
S32	110	(intellectual adj propertY IP) and (On adj Super-Sub IPOS) and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:55
S36	35	(intellectual adj propertY IP) and (On adj Super-Sub IPOS) and chip and @ad<"20020702"	USPAT	OR	ON	2006/06/09 17:57
S37	8	(intellectual adj propertY IP) with (On adj Super-Sub IPOS) with chip and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 17:58
S38	10	(intellectual adj propertY IP) and (On adj Super-Sub IPOS) and BIST and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 17:59
S39	40	(intellectual adj propertY IP) and (On adj Super-Sub IPOS) and scan and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 18:00

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S42	11	(intellectual adj propertY IP) and (On adj Super-Sub IPOS) and scan with (chain boundary) and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 18:03
S41	11	(intellectual adj propertY IP) and (On adj Super-Sub IPOS) and scan with (chain boundary) and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/09 18:03
S8	116	(intellectual adj propertY IP) and (On adj Super-Sub IPOS)	USPAT	OR	ON	2006/06/09 18:08
S48	166	(intellectual adj propertY IP logic) same boundary adj scan with controller and @ad<"20020702"	USPAT	OR	ON	2006/06/09 18:10
S47	11	(intellectual adj propertY IP logic) near3 boundary adj scan with controller and @ad<"20020702"	USPAT	OR	ON	2006/06/09 18:10
S45	109	(intellectual adj propertY IP logic) with boundary adj scan with controller	USPAT	OR	ON	2006/06/09 18:10
S46	97	(intellectual adj propertY IP logic) with boundary adj scan with controller and @ad<"20020702"	USPAT	OR	ON	2006/06/09 18:25
S50	12	(intellectual adj propertY IP logic) with boundary adj scan with controller and substrate and @ad<"20020702"	USPAT	OR	ON	2006/06/09 18:29
S52	1	(intellectual adj propertY IP logic) and boundary adj scan and controller near3 substrate and @ad<"20020702"	USPAT	OR	ON	2006/06/09 18:31
S53	13	(intellectual adj propertY IP logic) and boundary adj scan and controller with substrate and @ad<"20020702"	USPAT	OR	ON	2006/06/09 18:34
S54	2	"6,734,549"	USPAT	OR	OFF	2006/06/13 09:06
S1	1	"20040199840"	US-PGPUB; USPAT	OR	OFF	2006/06/13 09:06
S55	5	(US-7036058-$ or US-6430718-$ or US-6000051-$ or US-5321277-$ or US-6249893-$).did.	USPAT	OR	OFF	2006/06/13 09:15
S58	8	(intellectual adj propertY IP) and boundary adj scan with controller and substrate and @ad<"20020702"	USPAT	OR	ON	2006/06/13 09:18
S51	41	(intellectual adj propertY IP logic) and boundary adj scan with controller and substrate and @ad<"20020702"	USPAT	OR	ON	2006/06/13 09:18

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S49	19	(intellectual adj propertY IP logic) with boundary adj scan with controller and BIST and @ad<"20020702"	USPAT	OR	ON	2006/06/13 09:18
S60	2	(intellectual adj propertY IP) with boundary adj scan and controller and BIST and @ad<"20020702"	USPAT	OR	ON	2006/06/13 09:19
S61	12	(intellectual adj propertY IP) and substrate and boundary adj scan and controller and BIST and @ad<"20020702"	USPAT	OR	ON	2006/06/13 09:24
S57	4	S55 and (intellectual adj propertY IP core)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/13 10:52
S63	3	S55 and (intellectual adj propertY IP core) and substrate	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/13 10:53
S64	25	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) and TAP with controller and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/13 11:03
S29	4	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) with scan and controller and BIST and core and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/13 11:03
S65	3	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) with TAP with controller and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/13 11:05
S66	25	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) and TAP with controller and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/13 11:31
S67	23	(linear adj feedback adj shift adj register LFSR) with (multiple adj input adj signature adj register MISR) and TAP with controller and BIST and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/06/13 11:32
S62	40	(intellectual adj propertY IP) and substrate and boundary adj scan and controller and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:48

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S69	1	boundary adj scan with power adj supply near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:52
S68	10	substrate and boundary adj scan and power adj supply near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:52
S72	4	(multiple plurality) adj chips with power adj supply near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:54
S71	159	(multiple plurality) adj chips and power adj supply near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:54
S74	1	"714"/$.ccls. and (multiple plurality) adj chip and scan and power adj supply near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:55
S75	7	"714"/$.ccls. and (multiple plurality) adj chip and power adj supply near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:56
S78	4	boundary adj scan and (substrate board) with power adj supply near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 13:59
S82	4	integrated adj circuit with (substrate board) near3 power adj supply near control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:00
S81	71	integrated adj circuit and (substrate board) near3 power adj supply near control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:00
S85	110	integrated adj circuits with (substrate board) and power adj supply near control$3 and @ad<"20020702"	USPAT	OR	OFF	2006/06/13 14:01
S86	3	integrated adj circuits with (substrate board) same power adj supply near control$3 and @ad<"20020702"	USPAT	OR	OFF	2006/06/13 14:02
S88	3	ATE and UUT and power adj supply with control$3 and @ad<"20020702"	USPAT	OR	OFF	2006/06/13 14:03
S89	5	ATE with power adj supply with control$3 and @ad<"20020702"	USPAT	OR	OFF	2006/06/13 14:04
S93	1	ATE and (controllable programmalbe) adj power adj supply and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:05
S92	1	ATE and controllable adj power adj supply and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:05

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S94	14	ATE and (controllable programmable) adj power adj supply and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:06
S97	123	"714"/$.ccls. and JTAG and power adj supply and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:09
S95	40	"714"/$.ccls. and (controllable programmable) adj power adj supply and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:09
S99	19	"714"/$.ccls. and JTAG with (substrate board) and power adj supply and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:10
S98	78	"714"/$.ccls. and JTAG and (substrate board) and power adj supply and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:10
S101	96	boundary adj scan and supply with voltage with control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:15
S102	34	boundary adj scan and supply with voltage near3 control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:21
S105	123	714/735-745.ccls. and power near3 supply near3 voltage and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:27
S103	43	714/735-745.ccls. and power with supply with voltage with control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:27
S106	79	714/735-745.ccls. and power adj supply adj voltage and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:28
S107	18	714/735-745.ccls. and power adj supply adj voltage with control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:33
S108	7	TAP adj controller and power adj supply adj voltage with control$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 14:38
S109	25	TAP adj controller and power adj supply adj voltage and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:14
S115	495	power near sleep adj mode and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:15
S114	1087	power near3 sleep adj mode and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:15
S116	8	"714"/$.ccls. and power near sleep adj mode and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:16
S117	73	"714"/$.ccls. and power with sleep adj mode and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:17

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S119	1087	power near3 sleep adj mode and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:22
S118	23	"714"/$.ccls. and power near3 sleep adj mode and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:22
S120	21	under adj test and power near3 sleep adj mode and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:23
S122	219	under adj test and power adj off and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:24
S124	13	under adj test with power adj off and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:25
S126	371	under adj test and power adj control and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:43
S125	24	under adj test with power adj control and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:43
S127	14	under adj test and power adj control and test adj electronics and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:45
S129	12	power ADJ electronics with under adj test and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:46
S128	132	power ADJ electronics and under adj test and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:46
S132	209	"714"/$.ccls. and power with under adj test and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:52
S133	14	"714"/$.ccls. and boundary adj scan and power with under adj test and @ad<"20020702"	USPAT	OR	ON	2006/06/13 15:56
S134	19	"714"/$.ccls. and power near program$5 with under adj test and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:00
S136	2	"714"/$.ccls. and control$5 adj power adj supply and ATE and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:02
S135	21	"714"/$.ccls. and control$5 adj power adj supply and under adj test and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:02
S141	65	kerveros and wafer and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:07
S142	65	kerveros.xa. and wafer and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:09
S144	2	kerveros.xa. and (Farnworth.in. Wetsel.in.) and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:10
S143	2	kerveros.xa. and wafer and (Farnworth.in. Wetsel.in.) and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:10

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S146	2	kerveros.xa. and (Farnworth.in. Wetsel.in.) and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:11
S148	470	kerveros.xa.	USPAT	OR	ON	2006/06/13 16:12
S147	2	kerveros.xa. and (Farnworth.in. Wetsel.in.) and power and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:12
S151	470	"kerveros"	USPAT	OR	ON	2006/06/13 16:13
S137	3	"714"/$.ccls. and control$5 adj power adj supply and scan adj chain and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:14
S155	514	control$5 with power adj supply with wafer and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:22
S154	600	control$5 with power with supply with wafer and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:22
S152	30	"714"/$.ccls. and control$5 with power with supply and scan adj chain and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:22
S156	70	control$5 with power adj supply near3 wafer and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:23
S159	7	control$5 with power adj supply near3 wafer and test and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:30
S161	54	control$5 with power adj supply with chip with test$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:31
S162	39	(board substrate) and control$5 with power adj supply with chip with test$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:34
S164	2	(board substrate) and control$5 near3 supply adj voltage with chip with test$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:49
S163	12	(board substrate) and control$5 with power adj supply adj voltage with chip with test$3 and @ad<"20020702"	USPAT	OR	ON	2006/06/13 16:49
S130	19	power ADJ electronics same under adj test and @ad<"20020702"	USPAT	OR	ON	2006/10/30 10:08
S10	31	(intellectual adj propertY IP) and semiconductor with substrate and boundary adj scan	USPAT	OR	ON	2006/10/30 10:56
S166	6	(intellectual adj property IP) with (TAP controller) and semiconductor with substrate and boundary adj scan	USPAT	OR	ON	2006/10/30 11:00

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S168	4	(intellectual adj propertis IPs) and semiconductor with substrate and boundary adj scan	USPAT	OR	OFF	2006/10/30 11:10
S169	4	(intellectual adj properties IPs) and semiconductor with substrate and boundary adj scan	USPAT	OR	OFF	2006/10/30 11:11
S170	34	(intellectual adj property IPs) with (TAP controller) and boundary adj scan	USPAT	OR	ON	2006/10/30 11:12
S167	34	(intellectual adj property IP) and (TAP controller) and semiconductor with substrate and boundary adj scan	USPAT	OR	ON	2006/10/30 11:19
S171	35	(intellectual adj property IP) and semiconductor with substrate and boundary adj scan and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:25
S173	18	(intellectual adj property) and semiconductor with (substrate wafer) and boundary adj scan and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:37
S174	12	(intellectual adj property) and semiconductor with (substrate wafer) and boundary adj scan and bond$3 and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:39
S176	7	kerveros and (intellectual adj property) and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:40
S172	38	(intellectual adj property IP) and semiconductor with (substrate wafer) and boundary adj scan and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:41
S179	11	(intellectual adj property) with semiconductor with (substrate wafer) and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:42
S178	66	(intellectual adj property IP) with semiconductor with (substrate wafer) and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:42
S177	4533	(intellectual adj property IP) and semiconductor with (substrate wafer) and @ad<"20020702"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2006/10/30 11:42